



(19)

(11) Publication number:

03073567 A

Generated Document.

PATENT ABSTRACTS OF JAPAN

(21) Application number: 01210335

(51) Intl. Cl.: H01L 27/06 H01L 27/04

(22) Application date: 14.08.89

(30) Priority:

(43) Date of application
publication: 28.03.91(84) Designated
contracting states:

(71) Applicant: NEC CORP

(72) Inventor: KAMIOKA JUNJI

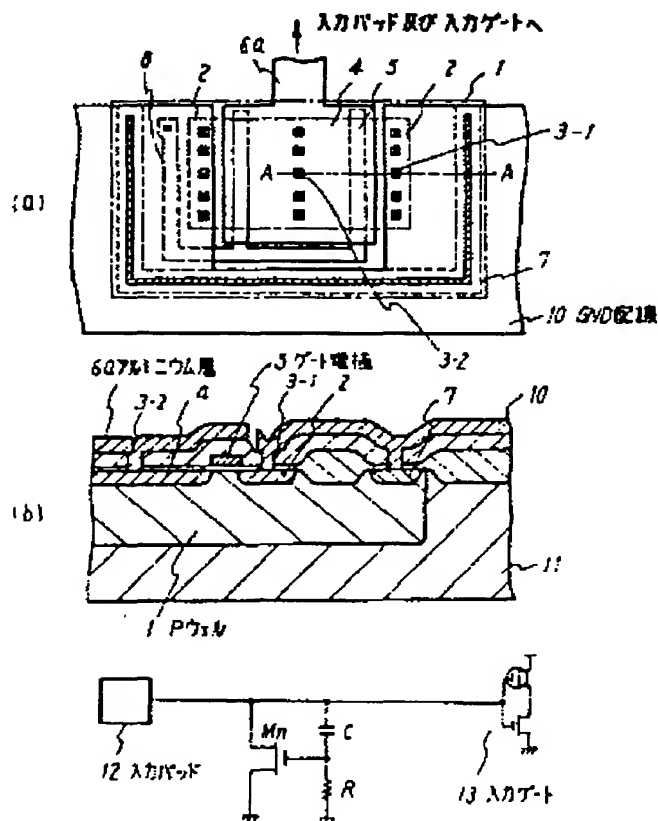
(74) Representative:

(54) INPUT PROTECTOR FOR
SEMICONDUCTOR
INTEGRATED CIRCUIT

(57) Abstract:

PURPOSE: To relieve concentration of electric field at the P-N junction of drain and to improve electrostatic breakdown strength by covering a gate electrode, inserted between an input pad and the input gate of inner circuit, with a conductive layer connected with the input pad thereby raising the potential at the gate electrode, upon application of positive voltage onto the input terminal, and conducting an nMOS transistor.

CONSTITUTION: A gate electrode 5 is connected through a polysilicon resistor 8 with GND wiring 10, and the N⁺ diffusion layer 4 in drain region is connected through a contact hole 3-2 with an aluminum film 6a. The aluminum film 6a is connected with an input pad and an input gate and applied onto the gate electrode 5 of an nMOS transistor, thus providing a coupling capacitance C between the aluminum film 6a and the gate polysilicon 5, and the nMOS transistor Mn is turned ON for a time interval determined by the product of the coupling capacitance C and the resistance R between the gate and the GND. Concentration of electric field at the P-N junction of drain is relieved through the



channel, resulting in the
improvement of electrostatic
breakdown strength.

COPYRIGHT: (C)1991,JPO&Japio